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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/594,561	09/27/2006	Kazumasa Tanida	AI-427NP	5593

23995 7590 05/18/2009

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EXAMINER	
OWEN, ROBERT W	

ART UNIT	PAPER NUMBER
2826	

MAIL DATE	DELIVERY MODE
05/18/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/594,561	TANIDA ET AL.	
	Examiner	Art Unit	
	ROBERT OWEN	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 September 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *27 February 2009*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Amendment filed on 27 February 2009.

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the insulating film having an opening greater in size than the semiconductor chip when the surface of the solid state device facing the semiconductor chip is viewed vertically from above must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering

of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the height of the pillar-shaped connecting member from the surface of the solid state device is approximately equal to a thickness of the insulating film must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New

Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the wiring between the solid state device and the semiconductor chip must be shown to be inside the wiring board and not on the top surface of the wiring board except for the connection pad or the feature(s) canceled from the claim(s). From a side view it is impossible to determine whether surface wiring exists behind the connecting member. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New

Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 3 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The specification (paragraph 19) states "A solder resist film 6 that has a thickness smaller than the interval between the surface 2a of the wiring board 2 and the semiconductor chip 3 is formed on the surface 2a." However, the specification does not indicate that the height of the pillar-shaped connecting member from the surface of the solid state device is approximately equal to the thickness of the insulating film.

Claim 5 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The specification (paragraph 4) states "The metallic balls 23 are re-wired inside the wiring board 22 and/or on the surface of the wiring board 22, and are electrically connected to a connecting member 5 on the side of the surface 22a." From this statement, it appears that there are two scenarios. In the first scenario, the metallic balls 23 are re-wired inside the wiring board 22 and on the surface of the wiring board 22. In the second scenario, they are re-wired inside the wiring board 22 or on the surface of the wiring board 22. The first and second scenarios do not indicate that the metallic balls are re-wired only inside the wiring board and not on the surface of the wiring board.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 4, 5, 6, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beddingfield et al. (U.S. Patent Number 5,710,071) in view of Tung

(U.S. Publication Number 2002/0033412 A1) and Urasaki et al. (U.S. Patent Numberr 6,281,450 B1).

In re claim 1, Beddingfield et al. (fig. 8) discloses a semiconductor device, comprising: a solid state device (30) (wiring substrate); a semiconductor chip (20) (die) having a functional surface on which a functional element is formed (column 4, lines 12-14) (integrated circuitry has been formed on the active surface of the die), the semiconductor chip (20) being bonded on a surface of the solid state device (30) with the functional surface (active surface of die 20) (column 4, lines 14-15) (the active surface includes solder bumps 22 for mounting to the substrate 30) thereof facing the surface of the solid state device (30) while maintaining a predetermined distance between the functional surface (active surface of die 20) thereof and the surface of the solid state device (30) (the distance between the functional surface and the surface of the solid state device is predetermined by the size and materials of the solder bump and the bonding conditions such as reflow temperature and compression); an insulating film (31) (solder mask) provided on the surface of the solid state device (30) facing the semiconductor chip (20), the insulating film (31) having an opening greater in size than the semiconductor chip (20) and a sealing layer (52) (underfill) that seals a space between the solid state device (30) and the semiconductor chip (20). However, Beddingfield does not disclose a pillar-shaped connecting member configured to connect the functional surface of the semiconductor chip to the surface of the solid state device and the insulating film having an opening greater in size than the semiconductor chip when the surface of the solid state device facing the semiconductor chip is viewed

from vertically above. Whereas Tung (fig. 2e, fig. 2f) discloses a pillar-shaped connecting member (16') (column 5, lines 28-30) (two elongated pillars 16' are formed comprising a copper portion 16a and a solder portion 16b') configured to connect the functional surface (fig. 1b) (column 4, lines 47-49) (circuits on the semiconductor die 12 are spaced apart from the solder portion 16b by the length of the portion 16a containing copper) of the semiconductor chip (12) (semiconductor die) to the surface of the solid state device (14) (substrate). A copper pillar is used to connect the die to the substrate because it is preferable that electronic devices and solder be separated by at least 55 microns (column 2, lines 4-5) in order to reduce the effect of particle emissions from solder (column 1, lines 30-31). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a pillar comprising a copper portion to connect the die to the substrate in place of the conductive bumps of Beddingfield such as taught by Tung in order to reduce the effect of particle emissions from solder on the die. Tung (fig. 1b) also teaches that the predetermined distance between the functional surface of the die (12) and the surface of the solid state device (14) is at least 75 microns (column 4, lines 62-63). Beddingfield and Tung do not disclose the insulating film having an opening greater in size than the semiconductor chip when the surface of the solid state device facing the semiconductor chip is viewed from vertically above. Whereas Urasaki (fig. 3a and fig. 3b) discloses the insulating film (6) (insulating coating) having an opening greater in size (column 4, lines 31-33) (boundary 2 of the insulating coating 6 is within a range of up to 300 um outward from the boundary 1 of the semiconductor chip mounting area) than the semiconductor chip

(3) when the surface of the solid state device (8) (substrate) facing the semiconductor chip (3) is viewed from vertically above. The insulating coating (6) is not directly adjacent to the semiconductor chip (3) because the surface of the substrate (8) near the boundary of the chip mounting area (1) is coated with an adhesive (9) for fixing the semiconductor chip (column 4, lines 28-30) on the substrate which also insulates the wiring conductors on the substrate (column 4, lines 34-36). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to form the insulating film of Beddingfield having an opening greater in size than the semiconductor chip when the surface of the solid state device facing the semiconductor chip is viewed from vertically above such as taught by Urasaki in order for the sustrate near the boundary of the chip mounting area to be coated with an adhesive for fixing the semiconductor chip on the substrate.

In re claim 2, Urasaki (fig. 3a and fig. 3b) discloses wherein the sealing layer (9) (adhesive) is provided in such a manner as to fill the opening (column 4, lines 31-33) (boundary 2 of the insulating coating 6 is within a range of up to 300 um outward from the boundary 1 of the semiconductor chip mounting area) with the sealing layer (9) (Column 4, lines 31-36) (if the distance between boundary 2 and boundary 1 exceeds 300um the wiring conductors on the substrate may not be completely covered by the adhesive 9).

In re claim 4, Tung (fig. 2e and fig. 2f) discloses wherein the pillar-shaped connecting member (16') is formed by bonding a connection pad (22) (contacts) provided on the solid state device (14) (substrate) and a projection electrode (16a and

16b') (column 5, lines 28-30) (pillars 16' comprise copper portion 16 and solder portion 16b') provided on the semiconductor chip (12) (die).

In re claim 5, Urasaki (fig. 2a and fig. 2b) discloses wherein no other wiring than a connection pad (5) (connecting terminals) for connection with the semiconductor chip (3) is provided on the solid state device (8) between the solid state device (8) and the semiconductor chip (3) (column 3, lines 16-20) (the area where the semiconductor chip is to be mounted may be designed such that connecting terminals 5 are provided only for the purpose of making connections to the bumps 4 of the semiconductor chip).

In re claim 6, Urasaki (fig. 3a and fig. 3b) discloses wherein a distance between an outer periphery (1) (boundary of the chip mounting area) of the semiconductor chip (3) and an edge (2) (boundary of the insulating coating) of the opening of the insulating film (6) (insulating coating) is 0.1 mm or more (column 4, lines 31-34) (boundary 2 of the insulating coating 6 is preferably within a range of up to 300 um from the boundary 1 of the semiconductor chip mounting area) when the surface of the solid state device (8) facing the semiconductor chip (3) is viewed from vertically above.

In re claim 7, Beddingfield (fig. 5) discloses wherein the semiconductor chip (20) (die) is connected in a flip chip manner (column 7, lines 2-3) (die 20 is mounted in a flip-chip configuration).

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Beddingfield et al. (U.S. Patent Number 5,710,071), Tung (U.S. Publication Number 2002/0033412 A1) and Urasaki et al. (U.S. Patent Numberr 6,281,450 B1) in view of Thompson et al. (U.S. Patent Number 5,218,234).

In re claim 3, Beddingfield, Tung, and Urasaki disclose the semiconductor device according to Claim 1 and Tung (fig. 1a and fig. 1b) discloses wherein the height of the pillar-shaped connecting member (16) is at least 75 microns such as in the range of about 80-100 microns (column 4, lines 62-64). In addition, Urasaki (fig. 3a and fig. 3b) discloses that the thickness of the insulating coating (6) is preferably 15 to 50 um, since thicker insulating coatings reduce productivity and elevate production cost (column 4, lines 43-51). However, Beddingfield, Tung, and Urasaki do not disclose wherein a height of the pillar-shaped connecting member from the surface of the solid state device is approximately equal to a thickness of the insulating film. Whereas Thompson (fig. 1) discloses wherein the thickness of the solder mask (24) is between about 0.5 mils (12.7 um) and about 10 mils (254 um) thick (column 5, lines 51-52). Thus, the height of the pillar-shaped connecting member (Tung fig. 1b) (16) from the surface of the solid state device (Tung fig. 1b) (14) disclosed by Tung to be at least 75 microns such as in the range of about 80-100 microns (Tung, column 4, lines 62-64) can be approximately equal to a thickness of the insulating film (solder mask). The solder mask (24) is formed on substrate (20) to insulate the conductive pattern (22) (column 2, lines 50-52) and an insulating film thicker than 50um enhances insulation reliability (Urasaki, column 4, lines 46-48). Therefore, it would have been obvious to one having ordinary skill in the art at

the time the invention was made for the thickness of the insulating film to be between about 80-100 microns so that it is approximately equal to the height of the pillar-shaped connecting member of Tung from the surface of the solid state device of Tung such as taught by Thompson and Urasaki in order to enhance insulation reliability.

Response to Arguments

Applicant's arguments filed 27 February 2009 have been fully considered but they are not persuasive. The above rejections address the Applicant's remarks regarding amended claims 1-2 and new claims 3-7.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT OWEN whose telephone number is (571) 270-7887. The examiner can normally be reached on Monday-Friday 8:30AM-6:00PM EDT.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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